Claim Amendments

Please amend claims 1 and 11 and as follows.

1. (currently amended) A method for increasing the strength of an electroplating cathode contact area on a semiconductor wafer to prevent insulating layer delamination comprising the steps of:

providing a semiconductor wafer comprising a periphery portion and a central portion comprising active chip portions;

providing a plurality of cathode contact areas within an exclusion region at the periphery portion of the semiconductor wafer excluding active chip portions said cathode contact areas comprising a cathode contact area insulating layer including a plurality of cathode contact area etched openings in closed communication with an underlying conductive region;

filling the cathode contact area etched openings with metal to form cathode contact area metal interconnects in electrical communication with [an] the underlying conductive region for electrical communication with a metal seed layer comprising the central portion;

planarizing an exposed surface of the cathode contact area metal interconnects; and,

forming a conductive layer over the cathode contact area metal interconnects to form a plurality of cathode contact pads for contacting a cathode for carrying out an electroplating process.

2. (original) The method of claim 1, further comprising the step prior to the filling step of depositing a barrier layer to cover at least the cathode contact area etched opening sidewalls and floors.

3. (original) The method of claim 2, wherein the barrier layer includes tantalum, tantalum nitride, titanium nitride, and combinations thereof.

4. (original) The method of claim 1, wherein the metal seed layer, the cathode contact area metal interconnects, and the contact pads comprise copper or an alloy thereof.

5. (original) The method of claim 1, wherein the cathode contact area metal interconnects comprise at least one of vias and trench lines.

6. (original) The method of claim 1, wherein the cathode contact area insulating layer comprises an insulating layer with a dielectric constant of less than about 3.0.

7. (original) The method of claim 1, wherein the cathode contact pads form a rectangular area from about 50 microns to about 150 microns on a side.

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8. (cancelled)

9. (previously presented) The method of claim 1, wherein the exclusion region comprises a circumferential edge of the semiconductor wafer extending about 1mm to about 3mm toward a central portion of the semiconductor wafer.

10. (previously presented) The method of claim 1, wherein the plurality of cathode contact pads are disposed to include the entire circumference of the semiconductor wafer.

11. (currently amended) A method for forming electroplating cathode contacts around the periphery of a semiconductor wafer comprising the steps of:

forming an insulating layer over a conductive layer comprising an exclusion region excluding active chip portions ~~around the~~ at a periphery portion of a semiconductor wafer substrate;

etching a plurality of openings ~~around~~ [a] within the ~~peripheral portion of the semiconductor wafer substrate~~ the exclusion region through the insulating layer to extend through a thickness of the insulating layer in closed communication with the conductive layer said conductive ~~area~~ layer in electrical

communication with a central portion of the semiconductor wafer substrate comprising active device areas;

filling the plurality of openings with metal to form electrically conductive pathways;

planarizing the electrically conductive pathway surfaces; and,

forming a metal layer over the electrically conductive pathway surfaces to form a plurality of contact pads for contacting a cathode for carrying out an electroplating process on a central portion of the semiconductor wafer comprising a damascene structure and a metal seed layer in electrical communication with the conductive layer.

12. (original) The method of claim 11, further comprising the step prior to the filling step of depositing a barrier layer to cover at least sidewalls and floors within the plurality of openings.

13. (original) The method of claim 12, wherein the barrier layer includes tantalum, tantalum nitride, titanium nitride, and combinations thereof.

14. (original) The method of claim 11, wherein the conductive pathways and the plurality of contact pads are selected from the group consisting of copper, aluminum, and tungsten.

15. (original) The method of claim 11, wherein the conductive pathways comprise at least one of vias and trench lines.

16. (cancelled)

17. (original) The method of claim 11, wherein the insulating layer comprises an insulating layer with a dielectric constant of less than about 3.0.

18. (original) The method of claim 11, wherein an individual contact pad forms a rectangular area from about 50 microns to about 150 microns on a side.

19. (previously presented) The method of claim 11, wherein the plurality of contact pads are disposed along a circumferential edge of the semiconductor wafer.

20. (cancelled)

21. (previously presented) The method of claim 1, wherein the cathode contact pads are formed to provide electrical communication through the underlying conductive region with a metal seed layer formed over the central portion.

22. (previously presented) The method of claim 21, wherein the metal seed layer comprises a portion of a damascene structure.